Industry Developments that Sustain the Growth of Crystalline Silicon PV Output

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Abstract

Reductions in silicon wafer thickness and kerf loss in the sawing process will lower silicon feedstock consumption to around 0.9 kg/m^2 by the year 2010. In combination with increased module efficiency, the PV output per kilogram of silicon feedstock should increase to around 160 Wp/kg. Together with increased production of polysilicon feedstock, the 2.5-fold increase in peak-Watt of output per kg silicon over the decade will continue to sustain the annual growth in PV.

Introduction

For more than 10 years the photovoltaic (PV) industry has sustained an average annual growth rate of over 30%, with even higher growth rates in recent years. These rates are projected to stay around 35% until 2010 and remain above 20% by 2015 [1]. Figure 1 shows the global PV output from 1995-2006 and the projected output over 2007-2025 anticipated by the European Photovoltaic Industry Association (EPIA) [1]. The inset in figure 1 shows detail of the crystalline silicon fraction in the decade 2000-2010.

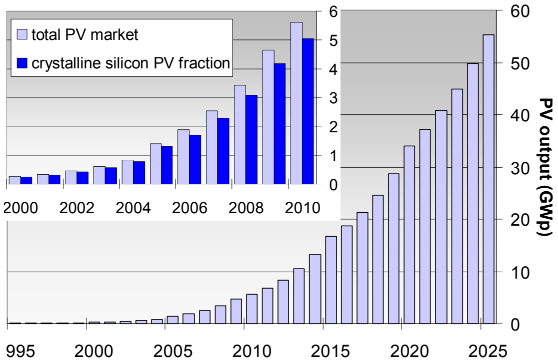

Figure 1. PV output growth as anticipated by EPIA [1] with inset showing crystalline silicon fraction over decade 2000-2010.

PV cell manufacture has been dominated by one cell technology with over 90% of the output based on crystalline silicon (c-Si) products. A breakdown of the global 2005 PV output by technology is given in figure 2.

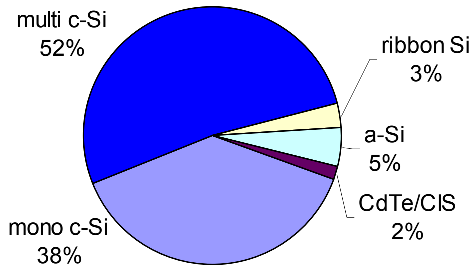

Figure 2. Breakdown of PV cell output by technology in 2005 [2].

The sustained growth rate and the dependence on a single high quality feedstock, shared with the microelectronics industry, have resulted in silicon shortages that have threatened to constrain the output growth. However, the industry has responded to this challenge by advancing techniques that result in more efficient use of feedstock and by developing high efficiency PV cells that increase the power output from each silicon wafer. This paper describes the most significant industry developments and the future expectations that should sustain the technology's market dominance for the next decade.

Silicon Wafer Production

Silicon is the second most abundant element on Earth, which provides a sound platform to sustain the long-term viability of the PV industry. However, a high purity silicon feedstock is required for PV cell manufacture. Metallurgical grade (MG) silicon is produced by the carbo-thermic reduction of quartz. This silicon is then reacted with hydrogen chloride to form tri-chlorosilane, which is purified by fractional distillation. The $SiHCl_3$ is then reduced with hydrogen to form the polysilicon feedstock used by the PV and microelectronics industries.
There are two main techniques used for the production of large silicon crystals from which wafers are fabricated for PV cells; *Multi*crystalline silicon growth by directional solidification in a quartz crucible (Ingot Casting) and *Mono*crystalline boule pulling by the

Czochralski (CZ) process. [Crystals are also made by Floating Zone (FZ) melting of polysilicon rod but this process is regarded as currently uneconomic for PV application].

Fixed cost reduction and sustained output growth has been achieved in recent years by increasing the size of cast ingots. The mass of the current industry ingot is typically 260 kg but ingots of up to 450 kg have been recently demonstrated [3]. Similarly, single CZ crystal pullers have increased in size and the latest generation pullers for PV are designed to grow 120 kg boules. These ingots and boules are cut into bricks that have the dimensions of the finished wafer (single crystal boules are machined square or have rounded corners). This brick sawing process uses large, high speed band saws where the kerf loss from sawing is typically 1.7 mm per cut. Over 11 kg of silicon is lost from each 260 kg ingot in the process of cutting 125 mm square bricks. New wire saw tools for brick cutting are beginning to enter service that use 0.25 mm diameter wire and reduce kerf loss to around 2 kg per ingot.

Both mono and multicrystalline bricks are sliced into wafers using wire saws. Each sawing cycle uses typically 240 km of steel wire of diameter of 160 μm. The wire is wound round a series of spools at a pitch of typically 400 μm. Using a cutting fluid comprising silicon carbide particles in mineral oil or ethylene glycol medium and a wire travelling between the spools at a speed of 12 m/s the bricks are sliced into wafers. Such a process produces silicon wafers of 200 μm thickness with an associated 50% silicon kerf loss. This process typically takes around 5.5 hours, simultaneously cutting 8 bricks and resulting in approximately 4200 wafers per run cycle. Significant advances have been made in this technology over recent years. Commercial trials are underway with smaller diameter wires of only 120 μm and used to cut wafers of thickness 150 μm or less that will result in a 30% higher wafer yield per kg of brick. It is anticipated that wafer thickness down to 100 μm or less will be commercially produced by this process. 80 μm thin wafers have been demonstrated by this process under laboratory conditions.

Feedstock Consumption

At the start of the decade (2000) the average crystalline silicon wafer used in PV cell manufacture was over 300 μm thick and required 2 kg/m^2 of high purity polysilicon feedstock to manufacture. Improvements to casting yield and greater recycling (*via* melt refining) of the silicon off-cuts from the ingot sizing process have produced significant silicon savings. The silicon wafer thickness has also been reduced to around 200 μm. These improvements have reduced silicon consumption per wafer to around 1.2 kg/m^2.

The recent developments in silicon sawing technology will see the introduction of commercial wire-saw tools for ingot sizing and smaller diameter wire in wafer sawing, both of which reduce silicon kerf loss. Wafer thickness is expected to reduce to 150 μm (perhaps 100 μm) over the next 5 years. In combination, these developments will reduce silicon feedstock consumption to around 0.9 kg/m^2. For the case of 125x125 mm^2 multicrystalline wafers, figure 3 illustrates the historic and projected reduction in feedstock consumption per wafer area (kg/m^2) over the decade 2000-2010 as a consequence of reduced wafer thickness, reduced kerf loss and increased recycling in the casting process. For the purpose of this calculation the wafer thickness was assumed to reduced linearly by 20 μm per year over the period 2000-2006 and will reduce by 12.5 μm per year from 2006-2010. Due to the increasing demand from PV, silicon feedstock prices started to rise significantly around the middle of the decade and, as a consequence, it became economically viable to recycle the off-cuts from the brick sizing process that contained high impurities (*e.g.* ingot tops). The impact of additional re-cycling on the feedstock consumption is noted in figure 3.

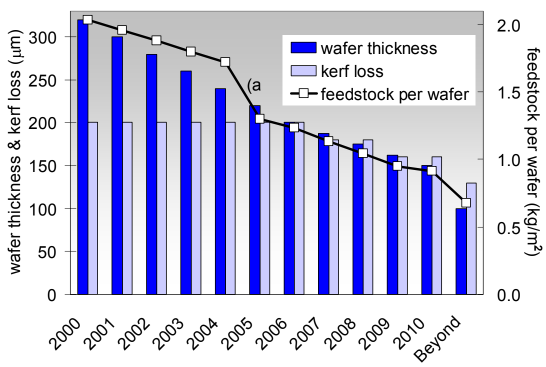

Figure 3. Silicon feedstock trend/projection from reduced wafer thickness, kerf loss and (a) increased recycling.

To calculate the feedstock consumption in figure 3 all process yields in wafer, cell and module production, were kept constant. In this calculation, the overall wafer yield from brick to module assembly is 78%, so there is scope for further reduction in silicon consumption through yield improvement but this will be a challenge as wafer thickness is reduced.

Cell and Module Performance

The most common PV cell is made with *p*-type silicon and has a typical efficiency of around 14-16% for multicrystalline wafers and 16-18% for monocrystalline wafers. However, there have been numerous advanced cell designs that result in significantly higher cell efficiency.

The first to be commercially produced in volume on *p*-type monocrystalline wafers was the laser grooved buried contact (LGBC) cell manufactured by BP Solar in Spain [4]. This cell was invented by Wenham and Green [5] at the University of New South Wales, Australia and features a selective emitter and copper plated contacts buried in grooves formed by laser micromachining. Over 20% cell efficiency has recently been demonstrated [6] for large area LGBC cells on thin wafers of only 140 μm thickness incorporating a laser-fired aluminium rear contact. A schematic cross-section of the cell structure is shown in figure 4.

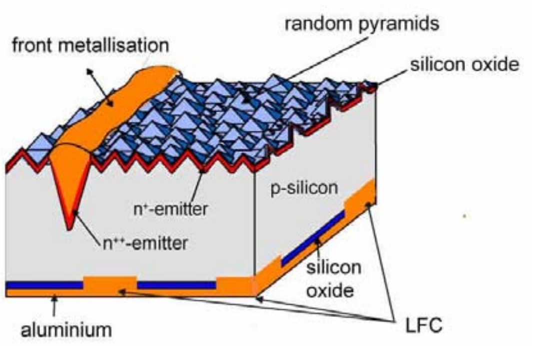

Figure 4. Schematic of the LGBC/LFC cell

In recent years two manufacturers have introduced high efficiency cells on *n*-type wafers; Sanyo demonstrated cells of up to 21.5% efficiency [7] and SunPower Corporation have also demonstrated a 21.5% efficient all rear contact cell [8].

In multicrystalline cell technology, Kyocera have recently demonstrated a cell efficiency of 17.7% [9]. Other leading cell manufacturers are likely to introduce competing technologies in the coming years that will increase the average industry efficiency.

Commercial module efficiencies are typically 2% points lower than bare cell efficiencies due to area-related losses from cell packing density and the module frame, absorption of the glass and losses in the cell interconnect ribbon. However, developments in module technology are closing this gap. BP Solar pioneered the commercial use of antireflection coated glass on solar modules achieving an efficiency gain of 2.4% under standard test conditions and a gain of 4% in energy conversion over the typical annual cycle [10].

Resistive power losses in the conductive ribbon used to interconnect cells in the module are significant and amount to some 11 Wp in a typical 180 Wp module. There are limits to the incorporation of thicker, less resistive ribbons in the module due to the stresses resulting from differential expansion between the soldered ribbon and silicon wafer. Multi-layer interconnect ribbons of aluminium and copper may allow thicker films to reduce internal resistive losses.

Impact of Consumption and Performance

The 35% per year market growth noted in the introduction will require significant industry investment in future feedstock production capacity. In calculating the future demand for silicon feedstock it is important to make due allowance for (i) technology advances that reduce the feedstock requirement per unit wafer area and (ii) the increases in cell efficiency. The industry metric commonly used for this parameter is the mass of silicon (in grams) per unit PV module power (in Watt-peak), *i.e.* g/Wp. For the case of 125x125 mm^2 multicrystalline wafers, figure 5 illustrates the historic and projected reduction in feedstock consumption per unit module power output (g/Wp) over the decade 2000-2010. For this calculation we have assumed a linear increase in cell efficiency of 0.4% pt per year over the period 2000-2005 and an increase of 0.3% pt per year from 2005-2010. The net impact of reduced feedstock consumption per wafer and higher efficiency results in an overall reduction in feedstock requirement per module Watt-peak from almost 16 g/Wp at the start of 2000 to 6 g/Wp by 2010 with the prospects of further reduction beyond 2010.

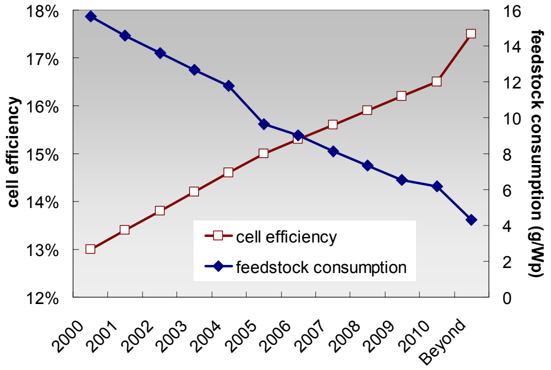

Figure 5. Trend and projection for multi c-Si cell efficiency and its impact on silicon feedstock consumption (g/Wp).

Using the unit feedstock requirement in figure 5 and the global market demand for crystalline silicon PV products in figure 1 we can calculate the future silicon feedstock requirements. Figure 6 shows the crystalline silicon PV output over the decade 2000-2010 (solid line/left hand axis) and the corresponding silicon requirement assuming the silicon g/Wp consumption at the start of the decade (solid light area/right hand axis). The dark shaded region in figure 6 shows the silicon feedstock requirement with the technology gains described in this paper and quantified in figure 5. It can be seen that the impact of the technology gains are substantial – reducing feedstock requirement in 2010 by over 60%. Whilst the compound annual growth rate in crystalline silicon PV over the decade 2000-2010 will be around 35% the required growth in silicon feedstock is only 24% due to technology advances.

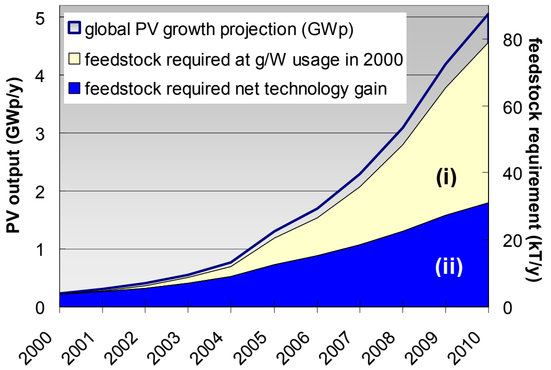

Figure 6. Feedstock required for market growth assuming (i) g/W consumption in 2000 and (ii) net requirement after technology advances

Conclusions

The implementation of technology developments by the PV industry including, increased silicon recycling, the introduction of wire saws for ingot sizing to bricks, reduced wafer thickness, reduced kerf loss in wafer slicing and higher cell and module efficiency will sustain the rapid growth of the PV industry in the near term. The combined impact of these developments over the decade 2000-2010 will:

- Reduce silicon feedstock consumption per wafer from 2.0 to 0.9 kg/m^2
- Increase Watt-peak output per kg of silicon feedstock from 60 to 160 Wp/kg (reduce requirement from 16 to 6 g/Wp)
- Require a compound annual silicon feedstock growth rate of 24% to fuel a market growth of 35% per annum.

References

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